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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/001,477	ROE ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-14 and 17-23 were rejected in the Office Action of 22 January 2007.

Applicants' submission filed on 26 April 2007 has amended claims 1, 7, 14, and 21-23. Claims 1-14 and 17-23 are pending in this application.

Claims 1-14 and 17-23 are rejected.

Priority

1. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Double Patenting

2. Claims 1, 7, and 14 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 13 of copending Application No. 09/975,338. Although the conflicting claims are not identical, they are not

patentably distinct from each other because where the limitations of claim 13 of the copending application only differ semantically from the independent claims 1, 7, and 14 of the instant application. Where claims from copending applications cover the same subject matter but are claimed slightly differently, it would have been obvious to a person of ordinary skill in the art to claim the invention in slightly different terms as exhibited the conflicting claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Applicants' response on 12 December 2005 states that Applicants will correspond to the provisional double patenting rejection upon an indication of allowance of subject matter of either the present application or the co-pending application (09/975,338).

Claim Rejections - 35 USC § 112

The previous rejections of claims 21-23 under 35 U.S.C. § 112, second paragraph, as being indefinite are withdrawn in response to the amendments thereto.

Response to Arguments

3. In response to the previous rejections of claims 1-14 and 17-23under 35 U.S.C. § 103 as being unpatentable over Marik in view of Grunert, Applicants argue primarily that:

> In contrast [to the language of claim 1], Marik discloses that the interrupt from the target system code to the interrupt handler debug routine is called "debugpoint" and that a table contains a record for each specified debugpoint in the target system (see Marik, col. 6, lines 51-55). Accordingly, Marik discloses that the table only contains the record of the debugpoint where interrupt is to occur. Therefore, portions of the target system code where debugpoint are not to occur are not included in the table. Accordingly, as acknowledged by the Examiner during the Examiner Interview on April 11, 2007, Marik fails to explicitly disclose the breakpoint lookup table comprising a plurality of break bits associated with a sequence of instructions addresses, and wherein each of the sequence of instruction addresses has a corresponding break bit, as claimed.

The Examiner respectfully traverses this argument as follows.

The claim language does not require break bits associated with instruction addresses where no break is to occur, as implied by Applicants' arguments. The relevant claim language merely recites "each of said sequence of instruction addresses has a corresponding break bit." This claim limitation requires a break bit for a sequence of instruction addresses, and to illustrate by contrast, does not recite "each instruction address in said sequence of instruction addresses has a corresponding break bit."

The recited claim language is taught by Marik where a user chooses to place a break bit at each instruction in a sequence of instructions. This would enable a person to perform debug operations (viewing register contents, viewing or altering memory contents, or altering debugpoints, etc.) subsequent to the execution of each instruction in the sequence. In this circumstance, Marik's debugpoint table clearly stores a debugpoint for each instruction in a sequence with a corresponding break bit. There is no requirement in the claim language to store break bits for instructions where no break is to occur.

Additionally, Marik expressly teaches that the "Boolean flag for breaking" may be set to "0"=disabled (column 6, line 67). Therefore, although there is no requirement for such a feature in the claim language, Marik expressly teaches "break bits associated with instruction addresses where no break is to occur."

4. Applicants further argue that:

> Marik teaches away from using in-circuit emulator technology, thereby fails to teach or suggest the in-circuit emulation system, as claimed.

The Examiner respectfully traverses this argument as follows.

Marik teaches a system that achieves the functionality of an in-circuit emulation system without additional "in-circuit emulator technology, additional microcontroller on-board circuitry, or a supporting microcontroller designed into the system under test" (column 2, lines 14-19). That is, the **object of Marik's invention is to enhance in-circuit emulation** by using fewer components. Marik plainly does not "teach away" from in-circuit emulation.

5. Applicants further argue that:

> The motivation of Grunert is a circuit arrangement for in-circuit emulation of a microcontroller (see Grunert, Title) to reduce the outlay for providing a microcontroller suitable for in-circuit emulation (see Grunert, col. 1, lines 35-36). Accordingly, even though the purpose of Grunert is to reduce the outlay for in-circuit emulation, it still requires in-circuit emulation. In contrast, as discussed above, Marik's motivation is to eliminate the in-circuit emulation technology altogether. In other words, the motivation behind Grunert is to use in_circuit emulation but with reduced outlay whereas the motivation for Marik as discussed above is to eliminate in-circuit emulator technology completely. As a result, one would not be motivated to combine the teachings of Marik with the teachings of Grunert.

The Examiner respectfully traverses this argument as follows.

As noted in Applicants' arguments, both Marik and Grunert are directed to improving in-circuit emulation technology by reducing the required components. A person of ordinary skill in the art with a desire to produce improved in-circuit emulator technology would be motivated to look to both of these references for what they teach as relevant to the problem at hand. The resulting invention would combine the advantageous teachings of both references. One possible motivation for combining the references has been explicitly set forth in the body of the rejection under 35 U.S.C. § 103.

6. Applicants submit arguments in favor of claims 3 and 10, but which refers back to and relies upon the language of claim 1. The arguments regarding the language of claim 1 have been addressed above.

7. Applicants further argue that:

> As per claim 5, the rejection relies on Grunert disclosing ports P5' and P6' where the result can be used for inputting and outputting further internal signals and states (e.g., control signals) (see Grunert, col. 5, lines 10-25). Moreover, the rejection relies on Grunert disclosing ports P3 and P4' where the internal states of the master and the slave can be transmitted (see Grunert, col. 5, liens 10-25). However, ports P5', P6', P3 and P4' are dedicated ports and are separate from one another. As a result, there is no two phase cycle, a control phase and a data transfer phase, as claimed, because the master and the slave have dedicated ports that can communicate and transfer data simultaneously, thereby eliminating the need for having any two phase cycle.

The Examiner respectfully traverses this argument as follows.

The claim language does not exclude dedicated ports. Further, although Grunert may disclose dedicated ports, Grunert does not explicitly disclose any simultaneous data transfer as described by Applicants. By the same type of analysis, Grunert may use the dedicated ports in a non-simultaneous fashion, and therefore teaches a two phase cycle.

8. Applicants further argue that:

> As per claim 21, the rejection asserts that Grunert discloses that the in-circuit emulation comprises two identical microcontrollers (see Grunert, col. 1, lines 48-51). Applicants do not understand identical structures to either teach or suggest that the content of the microcontroller can be accessed to reduce debugging related functions on the microcontroller, as claimed.

The Examiner respectfully traverses this argument as follows.

The language of claim 21 defines that "said virtual microcontroller functions identical to said microcontroller such that the content of said microcontroller can be accessed to reduce debugging related functions on said microcontroller." The prior art teaches the claimed virtual microcontroller functioning identically to the microcontroller. The claim language itself suggests that the content of the microcontroller can be accessed to reduce debugging related functions on the microcontroller.

The claim language does not require accessing content of said microcontroller, but merely that this access *can* occur.

Applicants' arguments have been fully considered but have been found unpersuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

9. Claims 1-14 and 17-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,903,718 to Marik in view of US Patent No. 6,366,878 to Grunert.

Regarding claim 1, Marik teaches:

An in-circuit emulation system [*"The Debug Tool of a preferred embodiment of the present invention is a 8031 debug tool with emulator types of functions which needs only a minicomputer, such as a PC, running a user-interactive PC Host Debugger Application program and a serial cable attaching the standard communication port of a PC to the 8031 based target system."* (column 3, line 66 – column 4, line 4)] breakpoint control [*"Debug Parameter Table"* (column 6, lines 48 *et seq.*)] comprising:

A microcontroller [*"According to the present invention, a remote program monitor method and system using a system-under-test microcontroller for self-debug comprises a system-under-test (SUT_ that includes a read-only memory (ROM) and a microcontroller for executing a program under test."* (column 2, lines 22-27)];

A breakpoint lookup table, wherein said breakpoint lookup table comprises a plurality of break bits associated with a sequence of instruction addresses, and wherein each of said sequence of instruction addresses has a corresponding break bit, the break bit being set to indicate that a break is to occur at a specified instruction address [*"The Debug Parameter Table contains a record for each specified debugpoint in the target system. Each record consists of: 1) A program memory address which is compared to the target system program counter at the time*

the debugpoint occurs. If a match occurs, the debugpoint takes action based upon the contents of the remainder of this record." (column 6, lines 48-61); in the claimed embodiment, a debugpoint would be established for each instruction in a sequence of instructions];

A breakpoint controller that sends a break message to the microcontroller whenever an instruction address is encountered that is associated with a set break bit [*"When the SUT receives one or more debugger signals as an interrupt input, the signal causes the microcontroller to execute a debugger program contained in the ROM."* (column 2, lines 22-38); *"When a debugpoint is reached, the INT0 interrupt handler checks the Debug Parameter Table to verify that the breakpoint is enabled. A break is enabled if the Break Boolean flag is set true and the program counter value in the Debug Parameter Table matches the program counter at the top of the stack upon entry into the INT0 interrupt handler."* (column 16, lines 19-35)].

Marik does not disclose a virtual microcontroller operating in lock-step synchronization with the microcontroller by virtue of their identical operation.

Grunert teaches a virtual microcontroller operating in lock-step synchronization with a microcontroller by virtue of their identical operation [*"The arrangement, according to the invention, for in-circuit emulation comprises two identical microcontrollers, which are operated as master and slave, as well as the external program memory. The slave receives the same program instructions parallel to the master."* (column 1, lines 47-65); *"In accordance with another feature of the invention, a clock synchronizes the two microcontrollers (2, 3)."* (column 2, lines 58-59)].

Grunert and Marik are analogous art because both are directed to microcontroller development and testing.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of the virtual microcontroller operating in lock-step synchronization with the teachings of Marik's debugging system to arrive at the claimed invention. The combination would involve the desirable features of Marik's debugging system with the desirable features of Grunert's virtual microcontroller system.

The motivation for doing so would be to achieve better visibility into the internal operations of the microcontroller, as expressly taught by Grunert [*"In accordance with an advantageous feature of the present invention, the operating program for in-circuit emulation is not stored in the internal ROM memory, but in an external, and therefore easily accessible memory."* (Grunert, column 1, lines 36-47); *"Internal states of the master 2 are transmitted to the slave 3 via the ports P3, P4', and then to the service computer via the ports P5', P6',.... The contents of the memory 4 can be changed by the service computer, in order to optimize the microcontroller in the application system during the development phase. The internal state of the master 2 can be traced by setting breakpoints. The service computer executes the application program in this case in parallel with the execution in the master 2."* (Grunert, column 5, lines 10-25)].

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the Marik and Grunert references to obtain the invention specified in claim 1.

Regarding claim 2, Grunert teaches that messages are sent to the microcontroller over an interface linking the (master) microcontroller to the (slave) virtual microcontroller [*"A signal connection between the microcontrollers 2, 3 is produced by port P3 in the master and port P4' in the slave. The respective settings of the connecting devices 9, 9' ensure that the ports P0', P2', P3' of the slave 3 are switched through to the master 2 so that all the input and output data of the function unit 7 are available in the master 2 as in normal operation."* (column 4, lines 63-67); *"The corresponding ports P5', P6' are therefore free in the slave 3, with the result that they can be used for inputting and outputting further internal signals and states, for example internal buses, control signals, register contents, etc. or for controlling the program execution.'"* (column 5, lines 10-25)].

Regarding claim 3, Marik teaches a counter that increments through the breakpoint lookup table as a sequence of instructions is executed [*"The Debugger Routine compares the program counter at the top of the stack upon entry into the INT0 Reentrant Routine with the program counter field of each record in the DPT until a match is found. If a match is found, the "active" DPT record is replaced by the new matched record. The debug Boolean flags in the DPT record dictate what action is to be taken."* (column 14, lines 59-65)]

Regarding claim 4, Marik teaches a host computer that programs the breakpoint lookup table to set a breakpoint bit at an instruction address where a break is to occur [*"To selectively disable or enable debugpoints, the PC host 10 can update the Debug Parameter Table of Boolean flags."* (column 15, line 50 – column 16, line 3); *"Initially, the target system 8031*

source code is assembled on the PC." (column 8, lines 4-22); *"Included in the assembly of the target system source code is the Debug Parameter Table and "enable INT0 interrupt" instructions placed at strategic locations where debugpoints are desired."* (column 8, lines 34-52)].

Regarding claim 5, Grunert teaches that the microcontroller and the virtual microcontroller operate in a two phase cycle comprising a control phase and a data transfer phase [control phase: *"The corresponding ports P5', P6', are therefore free in the salve 3, with the result that they can be used for inputting and outputting further internal signals and states, for example internal buses, control signals, register contents, etc. or for controlling the program execution."* (column 5, lines 10-25); data transfer phase: *"Internal states of the master 2 are transmitted to the slave 3 via the ports P3, P4', and then to the service computer via the ports P5', P6', ... The contents of the memory 4 can be changed by the service computer, in order to optimize the microcontroller in the application system during the development phase."* (column 5, lines 10-25)].

Regarding claim 6, Grunert teaches that the break message is sent during the control phase [*"The corresponding ports P5', P6', are therefore free in the salve 3, with the result that they can be used for inputting and outputting further internal signals and states, for example internal buses, control signals, register contents, etc. or for controlling the program execution."* (column 5, lines 10-25); *"The internal state of the master 2 can be traced by setting breakpoints."* (column 5, lines 10-25)].

Regarding claim 21, Grunert teaches that the microcontrollers are identical [*"two identical microcontrollers"* (column 1, lines 48-51)].

Claims 7-10, 12-13, and 22 recite combinations of limitations found in claims 1-6 and 21. As claims 1-6 and 21 are obvious over Marik in view of Grunert, claims 7-10, 12-13, and 22 are similarly obvious over Marik in view of Grunert.

Regarding claim 11, Marik teaches halting execution of instructions in the microcontroller prior to the instruction associated with the set break bit [*"When a debugpoint is reached, the INT0 interrupt handler checks the Debug Parameter Table to verify that the breakpoint is enabled... The INT0 routine will then invoke the Communication API to transfer the contents of the trace table to the PC host 10 for display, then query the Communication API for a message from the PC host 10 to continue processing the target system code 40."* (column 16, lines 19-35)].

Claims 14, 17-20, and 23 recite combinations of limitations found in claims 7-13 and 22. As claims 7-13 and 22 are obvious over Marik in view of Grunert, claims 14, 17-20, and 23 are similarly obvious over Marik in view of Grunert.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

US Patent No. 5,050,168 to Paterson teaches a breakpoint table as known and used in the prior art (FIG. 6; column 7, lines 5-34).

US Patent No. 6,681,280 to Miyake et al. teaches a breakpoint table as known and used in the prior art (FIG. 5; column 8, lines 39-48).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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